What is claimed is:

1. A data transfer control device for controlling data transfer between a first memory whose storage capacity is arbitrarily set and a second memory corresponding to a buffer memory incorporated in a peripheral module, said data transfer control device comprising:

a first register for storing a first value representing a first number of times for performing data transfer to suit a storage capacity of the second memory;

a second register for storing a second value representing a second number of times for performing data transfer to match an amount of transferring data stored in the first memory; and

a controller for controlling transferring of m-bit data (where 'm' is an integer arbitrarily set) based on the first value while controlling writing operations for the second memory, and for determining a timing to output an interrupt signal based on the second value with respect to a Central Processing Unit managing the first memory storing the transferring data.

2. A data transfer control device according to claim 1, wherein when a number of times for actually performing data transfer between the first memory and the second memory matches the second value set to the second register, the controller outputs the interrupt signal to the Central Processing Unit.

3. A data transfer control device according to claim 1, wherein a size of the second register is set in accordance with the storage capacity of the first memory.

4. A data transfer control device according to claim 2, wherein a size of the second register is set in accordance with the storage capacity of the first memory.

5. A data transfer control device according to claim 1, wherein the transferring data are sequentially transferred from the first memory to the second memory in accordance with a Direct Memory Access transfer.

6. A data transfer control device according to claim 1, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data.

7. A data transfer control method for controlling data transfer between a first memory whose storage capacity is arbitrarily set and a second memory corresponding to a buffer memory incorporated in a peripheral module, said data transfer control method comprising the steps of:

setting a first value representing a first number of times for performing data transfer to suit a storage capacity of the second memory;

setting a second value representing a second number of times for performing data transfer to match an amount of transferring data stored in the first memory;

controlling transferring of m-bit data (where 'm' is an integer arbitrarily set) based on the first value while controlling writing operations for the second memory; and

outputting an interrupt signal based on the second value with respect to a Central Processing Unit managing the first memory storing transferring data.

8. A data transfer control method according to claim 7, wherein the transferring data are sequentially transferred from the first memory to the second memory in accordance with a Direct Memory Access transfer.

9. A data transfer control method according to claim 7, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data.

10. A data transfer control method according to claim 7, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data, so that the n-byte data are collectively transferred from the first memory to the second memory by sequentially transferring the m-bit data the first number of times so as to satisfy the storage capacity of the second memory.

11. A data transfer control method according to claim 7, wherein the storage capacity of the second memory is set to store n-byte data (where 'n' is an integer arbitrarily set) comprising multiple sets of m-bit data, whereby when a number of times for actually transferring the m-bit data substantially matches a value calculated by dividing a total number of bits of the transferring data by 'm', the interrupt signal is output to the CPU.